CONTROLLERS DATASHEET

CPU800

Controller with redundant Ethernet ports

smar
Technology Company

CPU800 Controller with redundant Ethernet ports

TECHNICAL INFORMATION

Product Description

CPU800 module is the eighth generation of Smar Logic Controllers that include communication port and the ability to execute discrete control via ladder logic. In addition, the CPU800 controller has two Ethernet ports to ensure high availability of control and supervision, and also supports redundancy, providing the process with a high level of security.

Main Characteristics

Functionalities

- HSE Field Device
- Modbus Gateway (serial and TCP/IP)
- Ethernet connectivity

Technical Characteristics

- Two 10/100 Mbps Ethernet ports;
- 128 parameters can be linked externally via HSE links;
- Support Flexible Function Block (FFB);
- Discrete control via relay diagram;
- Access to I/O modules;
- Webserver;
- Modbus Gateway;
- Redundant operation;
- Real Time Clock (RTC) and watchdog;
- Supervision for up to 2000 points per second;
- It supports up to 16 HART modules (DF116/DF117).

Available Memory

Volatile Memory	8 Mbytes
Non Volatile Memory *	4 Mbytes
EEPROM	1 kbyte
Flash to the program	4 Mbytes
Flash to monitor	2 Mbytes

* It is kept by not rechargeable internal battery.

Discrete Control

In order to preserve customers investment, the CPU800 module accesses the same I/O cards used in the LC700 system. Through the IMB (Inter-Module Bus), present in the rack where the CPU module is mounted, up to 16 racks R-700-4A or DF93 can be interconnected, each containing up to 4 cards. In case you have a redundant controller, the DF92 rack should be used. If DF92 is used, another 16 DF93 racks can be used. Additionally, there may be a need for other power supplies depending on the number of cards.

DF Line of I/O cards that can be used

Digital inputs and outputs
Analog inputs and outputs
Temperature
Pulse counting

The user program is developed using relay diagrams (IEC-61131-3), through the LogicView for FFB tool, available on System302. The LogicView for FFB is a complete development environment, allowing the user to create, edit, simulate and supervise the developed application. The interconnection with fieldbus is made through a flexible function block.

General Characteristics of the discrete control in the CPU800

I/O Points *	Maximum 1024 discrete points or 512 analog points
Auxiliary Points	Maximum of 4096 points
Ladder Function Blocks	Maximum of 2000 blocks **
Configuration File	Maximum 120 kbytes
Program run cycle for every 1000 Boolean operations (without redundancy)	10 ms (minimum)*** 32 ms (typical)****
Program run cycle with redundancy enabled	Adding to the run cycle From 10 ms (typical)***** and up to 50 ms (maximum)
Program Run Time	1.1 ms/Kbyte of program (minimum) 3.7 ms/Kbyte of program (typical)

* Total set of points including inputs and outputs, digital and analog. Maximum quantity may vary depending on the type of I/O hardware used.
** 120 kbytes and 2000 blocks available from firmware version 2.x. Previous versions support 60 Kbytes and 1200 blocks respectively.
*** Flexible block priority 1131 set to Zero (Very high priority), not using blocks and HSE links. Each 1000 Boolean operations use 8.6 Kbytes.
**** Total run time will vary depending on the adjusted priority of the task executing flexible block 1131. It must be compatible with the number of blocks and HSE links.
***** Total transfer time will be proportional to the program size.

The extensive library of LogicView for FFB function blocks allow the implementation of discrete and/or continuous control.

The complete list can be seen in the LogicView for FFB manual available on the Smar website.

The size of the configuration file and its time of execution can be estimated through a simple addition of the elements that compose the program. The total execution time will be given by the configuration execution time plus the program execution cycle, that is 10ms.

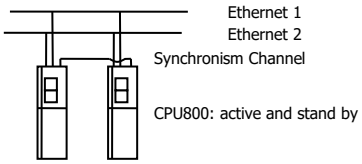
Redundant Operation

CPU800 can operate in standalone (one CPU800) or redundant (two CPU800) mode. In redundant mode, the two CPU800 are capable to communicate through a proprietary channel and change information about configuration and operation status.

Some CPU800 elements are redundant:

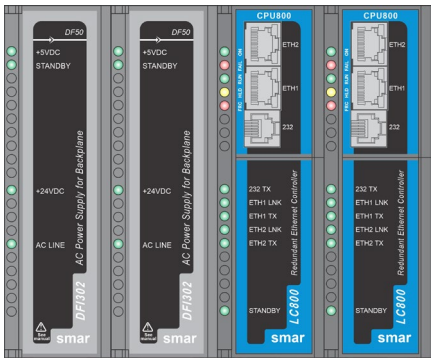
- HSE Block Redundancy
- HSE link Redundancy
- Ladder Redundancy
- Supervision Redundancy
- Ethernet Media Redundancy

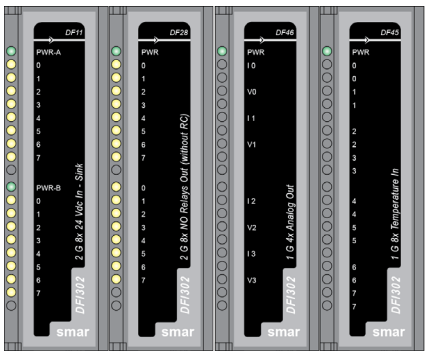
Topology to interconnection of CPU800 in redundancy:



Redundancy General Characteristics

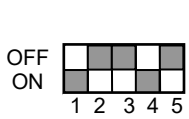
For redundancy of access in I/O cards, it is necessary the use of a special rack (DF78 or DF92). The two power supplies and the two CPU800 must be mounted on this rack, in that order. The remaining modules can be interconnected as usually.





Internal Battery

The CPU800 Real Time Clock (RTC) and its non volatile RAM (NVRAM) are maintained by a non-chargeable battery when there is lack of external supply. This battery can be either enabled or disabled, depending on the position of the switch 1, in the back part of the CPU800. To enable the battery, let the switch 1 as the following picture:



1) Battery ON
2) Keep in this position
3) Simulate
4) Watchdog ON
5) Keep in this position

In this configuration, when there is lack of energy, the RTC and the NVRAM will be supplied by the battery, allowing the retention of all configuration data. In case of equipment storage, it is recommended that the battery is turned off (switch 1 in position OFF).

Battery features

Type of battery	Battery Panasonic BR-2/3AE2SP - Lithium
Capacity	1200 mAh
Devices maintained by the battery	RTC and NVRAM
Minimum life span	8 years (typical charge of 17uA)
Maximum life span	49 years (typical charge of 2.8uA)
Voltage	3 V (subject to revision when below 2.5 V)

Ports and Communication Channels

Ethernet Port

Communication rate	10/100 Mbps
Standard	IEEE 802.3u
Isolation	150Vrms
Operation Mode	Full-duplex
Connector	RJ45 with shield*

* Grounded to the rail used for fixing the rack in which the CPU800 is installed.

Modbus Port

Maximum Communication Rate*	115200 bps
Standard	EIA-232
Connector **	RJ12 with shield
Maximum Current ***	0.5A @ 3.3V

* There is an increase in the error rate as we increase the communication rate above 19200 bps. In many situations these errors may be acceptable and not perceived by supervision.
** Grounded on the rack rail that is installed the CPU
*** Internally protected by solid state fuse

Redundant Port

Maximum Communication Rate	115200 bps *
Standard	EIA-232
Connector	RJ12 with shield**
Maximum Current***	0.5A @ 3.3V

* Rate for control information. Data traffic through Ethernet.
** Grounded to the rail used for fixing the rack in which the CPU800 is installed.
*** Internally protected by solid state fuse.

Failure Relay

Output type	Solid state relay, normally closed (NC), isolated
Maximum Voltage	30 VDC
Maximum Current	200 mA
Overload Protection	Not available. Must be provided externally
Normal Operation	Open contacts
Failure Condition	Closed contacts
Maximum cable length connected to the relay	30m

The load power supply driven by the fail relay must not be from a network outside the panel.

IMB Bus

Voltage	5 VDC
Bus	8 bits
Failure Signal	Yes
Hot Swap	Yes
Redundancy in the bus access	Yes, but only using DF78 or DF92 rack

Module Features:

Processor

CPU	Family ARM7TDMI
Bus	32bits
Architecture	RISC
Performance	40 MIPS
CPU Cache	8kbytes
Clock	40 MHz
DMA	10 channels
Ethernet	MAC 10/100 integrated
Watchdog	Yes (200ms of cycle)
Operation Voltage	3.3V for I/O

Module

Operation Voltage	5V (± 5% of tolerance)
Typical Current	550 mA
Real Consumption	2.75 W
Environment Air Temperature (Operation)	0 to 60º C (IEC 1131)
Storage Temperature	-20 to 80º C (IEC 1131)
Relative Air Humidity (Operation)	5% to 95% (non-condensing)
Cooling Mode	Air Convection
Dimensions (HxWxD, mm)	149x40x138 (without package)

Electrical Certification

CPU800 follows the immunity test specification to equipment to industrial installation, as IEC61326:2002 standard.

Enclose

Electrostatic discharge (IEC61000-4-2)	4 kV/8 kV contact/air
EM field (IEC61000-4-3)	10 V/m
Rated power frequency magnet field (IEC61000-4-8)	30 A/m

AC power

Voltage dip/short interruptions (IEC61000-4-11)	0.5 cycle, each polarity/100%
Burst (IEC61000-4-4)	2 kV
Surge (IEC61000-4-5)	1 kV/2 kV
Conducted RF (IEC61000-4-6)	3 V

DC power

Burst (IEC61000-4-4)	2 kV
Surge (IEC61000-4-5)	1 kV/2 kV
Conducted RF (IEC61000-4-6)	3 V

I/O signal/control

Burst (IEC61000-4-4)	1 kV
Surge (IEC61000-4-5)	1 kV
Conducted RF (IEC61000-4-6)	3 V

I/O signal/control connected directly to power supply network

Burst (IEC61000-4-4)	2 kV
Surge (IEC61000-4-5)	1 kV/2 kV
Conducted RF (IEC61000-4-6)	3 V

Emission Rate

Enclose

30 to 230 MHz (CISPR 16-1, CISPR 16-2)	40 dB (uV/m) quasi peak, measured at 10m distance
239 to 1000 MHz (CISPR 16-1, CISPR 16-2)	40 dB (uV/m) quasi peak, measured at 10m distance

AC mains

0.15 to 0.5 MHz (CISPR 16-1, CISPR 16-2)	79 dB (uV) quasi peak 66 dB (uV) average
0.5 to 5 MHz (CISPR 16-1, CISPR 16-2)	73 dB (uV) quasi peak 60 dB (uV) average
5 to 30 MHz (CISPR 16-1, CISPR 16-2)	73 dB (uV) quasi peak 60 dB (uV) average

Note: For most recent updates, please consult Smar **website www.smar.com.**

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